COPY

PATENT
Atty. Dkt. No. SAR14179

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Avery et al.

Patent No.: 6,791,122 B2

Issued: September 14, 2004

Serial No.: 10/007,833

Filed: November 5, 2001

Group Art Unit: 2826

Examiner: Tran, Tan N

For: SILICON CONTROLLED RECTIFIER ELECTROSTATIC DISCHARGE PROTECTION DEVICE WITH EXTERNAL ON-CHIP TRIGGERING AND COMPACT INTERNAL DIMENSIONS FOR FAST TRIGGERING

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

CERTIFICATE OF MAILING
37 CFR 1.8

I hereby certify that this correspondence is being deposited on 9/30/04 with the United States Postal Service as First Class Mail in an envelope addressed to: Certificate of Correction Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

9/30/04
Date

Signature

REQUEST FOR CERTIFICATE OF CORRECTION

Attached is a Certificate of Correction for correcting errors in the printed patent. The Applicants submits that the errors mentioned above were not made by the Applicants, but were made during the printing of the patent. The amended text in the specification can be found in the patent application as originally filed on November 5, 2001. The amended text in the claims can be found in the Applicant's response, dated August 29, 2003, to the Final Office Action dated May 29, 2003. A copy of the Applicant's response is attached. The amendments to the drawings can be found in the Applicant's response, dated October 3, 2002, to the Office Action dated, July 3, 2002. Accordingly, the Applicants believe that no fee is due for the certificate of correction. However, if fees are due, the Commissioner is hereby authorized to charge

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counsel's Deposit Account No. 20-0782 for any fees required to make this response acceptable to the Office.

Respectfully submitted,

9/30/04

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO: US 6,791,122 B2

DATED: September 14, 2004

INVENTOR(S): Leslie R. Avery, Christian C. Russ, Koen G. M. Verhaege, Markus P. J. Mergens, John Armer

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Figure 1A.
Please change reference numeral "125" to -- 129 --.

Figure 1B
Please change reference numerals "125", "241" and "242" to -- 129 --, -- 141 -- and -- 142 --, respectively.

Figure 2(A)-(D)
Please add reference numeral -- 136 -- at the first gate of transistor T1.

Column 11
Line 30, please change "^{318}A" to -- 318_{A} --.

Column 16, Claim 1,
Line 56, please change "arid" to -- and --.

Column 16, Claim 3,
Line 67, please change "translstor" to -- transistor --.

Column 17, Claim 3
Line 3, please change "lowing" to -- forming --.

Column 17, Claim 6
Line 12, please change "firs'" to -- first --.

Column 17, Claim 6
Line 13, please change "0.8 to 0.8" to -- 0.6 to 0.8 --.

Column 17, Claim 7
Line 16, please change "typo" to -- type --.

Column 17, Claim 8
Line 18, please change "ESO" to -- ESD --.

Column 17, Claim 11
Line 34, please change "In" to -- in --.

Column 17, Claim 11
Line 35, please change "N-wall, at least two cascaded" to -- N-well, at least two cascoded --.

Column 17, Claim 15
Line 63, please change "pad end" to -- pad and --.

Column 17, Claim 16
Line 65, please change "ESO" to -- ESD --.

Column 18, Claim 20
Line 11, please change "MOS PET" to -- MOSFET --.

Column 18, Claim 22
Line 22, please change "In" to -- in --.

Column 18, Claim 24
Line 33, please change "P-will" to -- P-well --.

Column 18, Claim 24
Line 33, please change "In" to -- in --.

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PATENT No. 6,791,122 B2
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IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

PATENT APPLICATION

Applicant: Avery, et al. Case: SAR 14179

Serial No.: 10/007,833 Filed: November 5, 2001

Examiner: Tran, Tan N. Group Art Unit: 2826

Title: **SILICON CONTROLLED RECTIFIER ELECTROSTATIC DISCHARGE PROTECTION DEVICE WITH EXTERNAL ON-CHIP TRIGGERING AND COMPACT INTERNAL DIMENSIONS FOR FAST TRIGGERING**

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RESPONSE UNDER 37 C.F.R. §1.116

S I R:

In response to the Final Office Action dated May 29, 2003 (Paper No. 7), please consider the discussion herein for the above-identified patent application as follows:

IN THE CLAIMS

Current status of all of the claims of the present application is listed below as follows:

1. (Previously Presented) An electrostatic discharge (ESD) protection circuit in a semiconductor integrated circuit having protected circuitry, the ESD protection circuit comprising:

a silicon controlled rectifier (SCR) having an anode coupled to the protected circuitry and a cathode coupled to ground, said cathode having at least one first high-doped region;

at least one trigger-tap, disposed proximate to the at least one high-doped region; and

an external on-chip triggering device coupled to the trigger-tap and the protected circuitry.

2. (Previously Presented) The ESD protection circuit of claim 1, further comprising a lateral shunt resistor coupled between the cathode and the external triggering device.

3. (Original): The ESD protection circuit of claim 1, wherein the SCR comprises a first bipolar transistor T1 and a second bipolar transistor T2; said first bipolar transistor having the at least one first high doped region serving as an emitter and forming the cathode, a first low doped region coextensively forming a base of the first bipolar transistor T1 and a collector of the second bipolar transistor T2, a second low doped region coextensively forming a base of the second bipolar transistor T2 and a collector of the first bipolar transistor T1, and a second high doped region serving as an emitter of the second bipolar transistor T2 and forming the anode.

4. (Previously Presented) The ESD protection circuit of claim 3, wherein a surface area between the respective first and second high-doped regions of the first and second bipolar transistors are blocked from shallow trench isolation.

5. (Original) The ESD protection circuit of claim 3, wherein the bases of the first and second transistors have base widths less than 4.0 microns.

6. (Original) The ESD protection circuit of claim 5, wherein the bases of the first and second transistors have base widths in a range of 0.6 to 0.8 microns.

7. (Original) The ESD protection circuit of claim 3, wherein the at least one first high doped region is a N+ type material, the first low doped region is a P-type material, the second low doped region is a N-type material, and the second high doped region is a P+ type material.

8. (Original) The ESD protection circuit of claim 7, wherein the triggering device is a MOSFET transistor selected from the transistor group consisting of a NMOS, a NMOS provided with drain-bulk-gate coupling, a NMOS in an isolated P-well, at least two cascoded NMOS transistors, and a ballasted NMOS.

9. (Previously Presented) The ESD protection circuit of claim 8, wherein a source and a drain of the MOSFET transistor are respectively coupled to the trigger-tap and to the protected circuitry.

10. (Previously Presented) The ESD protection circuit of claim 9, wherein a gate of the MOSFET is coupled to the source of the MOSFET transistor selected from the transistor group consisting of the NMOS, the NMOS in an isolated P-well, the at least two cascoded NMOS transistors, and the ballasted NMOS.

11. (Original) The ESD protection circuit of claim 7, wherein the triggering device is a MOSFET transistor selected from the transistor group consisting of a PMOS, a PMOS provided with drain-bulk-gate coupling, a PMOS in an isolated N-well, at least two cascoded PMOS transistors, and a ballasted PMOS.

12. (Previously Presented) The ESD protection circuit of claim 11, wherein a drain and a source of the MOSFET transistor are respectively coupled to the trigger-tap and the protected circuitry.

13. (Previously Presented) The ESD protection circuit of claim 12, wherein a gate of the MOSFET is coupled to the source of the MOSFET transistor selected from the transistor group consisting of the PMOS, the PMOS in an isolated N-well, the at least two cascoded PMOS transistors, and the ballasted PMOS.

14. (Original) The ESD protection circuit of claim 3, wherein a surface area between the respective first and second high-doped regions of the first and second bipolar transistors are shallow trench isolated.

15. (Previously Presented) An electrostatic discharge (ESD) protection circuit in a semiconductor integrated circuit (IC) having protected circuitry, the ESD protection circuit comprising:

a SCR further comprising:

a substrate;

a N-well and an adjacent P-well formed in said substrate and defining a junction therebetween;

at least one N+ doped region in said P-well and coupled to ground;

a P+ doped region in said N-well and coupled to a pad of said protected circuitry;

at least one P+ doped trigger tap disposed proximate to at least one N+ doped region in said P-well; and

an external on-chip triggering device coupled to the SCR, wherein one terminal is coupled to the pad and a second terminal is coupled to the trigger tap.

16. (Original) The ESD protection circuit of claim 15, wherein the second terminal is further coupled to ground via a shunt resistor.

17. (Previously Presented) The ESD protection circuit of claim 15, wherein a surface area between the at least one N+ doped region and the P+ doped region is shallow trench isolation blocked.

18. (Original) The ESD protection circuit of claim 15, wherein respective base widths between the P+ doped region and the junction, and between the at least one N+ doped region and the junction are less than 4.0 microns.

19. (Original) The ESD protection device of claim 15, wherein a P-well-tie is coupled to the P-well and grounded.

20. (Original) The ESD protection circuit of claim 15, wherein the triggering device is a MOSFET transistor selected from the transistor group consisting of a NMOS, a NMOS provided with drain-bulk-gate coupling, a NMOS in an isolated P-well, at least two cascoded NMOS transistors, and a ballasted NMOS.

21. (Previously Presented) The ESD protection circuit of claim 20, wherein a source and a drain of the MOSFET transistor are respectively coupled to the trigger-tap and the pad.

22. (Previously Presented) The ESD protection circuit of claim 21, wherein a gate of the MOSFET is coupled to the source of the MOSFET transistor selected from the transistor group consisting of the NMOS, the NMOS in an isolated P-well, the at least two cascoded NMOS transistors, and the ballasted NMOS.

23. (Original) The ESD protection circuit of claim 15, wherein a surface area over a non high-doped region and between the P+ doped region and the at least one N+ doped region is fully shallow trench isolated.

24. (Previously Presented) An electrostatic discharge (ESD) protection circuit in a semiconductor integrated circuit (IC) having protected circuitry, the ESD protection circuit comprising:

a SCR further comprising:

a substrate;

a P-well and an adjacent N-well formed in said substrate and defining a junction therebetween;

at least one P+ doped region dispersed in said N-well;

a N+ doped region dispersed in said P-well and coupled to ground;

at least one N+ doped trigger tap disposed proximate and between the at least one P+ doped region in said N-well; and

a PMOS transistor triggering device coupled to the SCR, wherein a drain is coupled to ground and a source is coupled to the trigger tap; the at least one P+ doped region is further coupled to a pad; the source is further coupled to the pad via a shunt resistor; and the pad is further coupled to said protected circuitry.

25. (Original) The ESD protection circuit of claim 24, wherein a surface area over a non-high-doped region and between the at least one P+ doped region and the N+ doped region is shallow trench isolation blocked.

26. (Original) The ESD protection device of claim 24, wherein a N-well tie is coupled to the N-well and coupled to the pad.

27. (Original) The ESD protection circuit of claim 24, wherein the triggering device is a PMOS transistor selected from the transistor group consisting of a PMOS, a

PMOS provided with drain-bulk-gate coupling, a PMOS in an isolated N-well, at least two cascoded PMOS transistors, and a ballasted PMOS.

28. (Previously Presented) The ESD protection circuit of claim 27, wherein a source and a drain of the MOSFET transistor are respectively coupled to the at least one trigger-tap and ground.

29. (Previously Presented) The ESD protection circuit of claim 28, wherein a gate of the MOSFET is coupled to the source of the MOSFET transistor selected from the transistor group consisting of the PMOS, the PMOS in an isolated N-well, the at least two cascoded PMOS transistors, and the ballasted PMOS.

30. (Original) The ESD protection circuit of claim 24, wherein respective base widths between the N+ doped region and the junction, and between the at least one P+ doped region and the junction are less than 4.0 microns.

31. (Original) The ESD protection circuit of claim 24, wherein a surface area over a non high-doped region and between the N+ doped region and the at least one P+ doped region is fully shallow trench isolated.

REMARKS

In the Office Action, the Examiner noted that claims 1-31 are pending in the application, of which claims 1-3, 5-8, 11, 15, 16, and 18-20 stand rejected, claims 24-31 have been allowed, and claims 4, 9, 10, 12-14, 17, and 21-23 stand objected to. By this response, claims 1-31 continue unamended. The Applicants thank the Examiner for indicating the allowable subject matter with respect to claims 24-31.

In view of the following discussion, Applicants submit that none of the claims now pending in the application are anticipated under the provisions of 35 U.S.C. §102 or obvious under the provisions of 35 U.S.C. §103. Thus, Applicants believe that all of these claims are now in condition for allowance.

OBJECTIONS

A. ALLOWABLE SUBJECT MATTER

The Examiner has objected to claims 4, 9, 10, 12-14, 17, and 21-23 as being dependent upon a rejected base claim. The Examiner concludes that these claims would be allowable subject matter if rewritten in independent form including all the limitations of the base claim and any intervening claims.

The Applicants thank the Examiner for indicating the allowable subject matter with respect to these claims. However, in view of the arguments set forth herein, the Applicants believe base claims 1 and 15 (and all intervening claims) are in allowable form and, as such, the dependent claims 4, 9, 10, 12-14, 17, and 21-23, as they stand, are therefore in allowable condition. Therefore, the Applicants respectfully request that the foregoing objections to these claims be withdrawn.

REJECTIONS

A. 35 U.S.C. §102

1. Claims 1 and 2

The Examiner rejected claims 1 and 2 as being anticipated by Russ (United States patent publication 2002/0041007, published April 11, 2002, hereinafter referred to as the "Russ publication"). The rejection is respectfully traversed.

The Examiner has cited, as the basis for rejecting claims 1 and 2 the Russ publication, entitled "Multifinger Silicon Controlled Rectifier Structure For Electrostatic Discharge Protection". The Russ publication was filed on October 10, 2001 and subsequently published on April 11, 2002. The Applicants submit that they conceived and reduced their invention to practice, as presently claimed, prior to the publication date of the Russ publication. In support of this submission, the Applicants enclose herewith a declaration under 37 CFR §1.131 that has been executed by the available inventors, which declares a conception date for the invention claimed in the above-identified patent application to be on or before October 10, 2001, and that due diligence was exercised towards reducing the invention to practice.

In particular, the Applicants have enclosed herewith, various copies of documents (Exhibits A-E) that provide evidence of an earlier invention date. It is noted that the Applicants have modified the Exhibits A-E by removing reference dates thereon. The Applicants will submit unmodified copies of the Exhibits A-E if deemed necessary. In view of this declaration, the Russ publication may no longer be considered as a prior art reference with respect to the Applicants' invention.

Further, as stated in MPEP 715.04, a declaration filed under Rule 37 CFR 1.131 requires the signature of each of the joint inventors, unless it is shown that an inventor or inventors were "otherwise unavailable." In that instance, the signatures of the remaining inventors are sufficient. It is noted that inventors Christian C. Russ and Markus P.J. Mergens are unavailable to execute the enclosed declaration. Mr. Russ and Mr. Mergens have moved to Germany and are both unavailable to execute the declaration. However, the available inventors, Leslier R. Avery, John Armer, and Koen G.M. Verhange have executed the enclosed declaration to fulfill the requirements under MPEP 715.04. As such, the Applicants respectfully request that this declaration be entered and judged effective as swearing behind the Russ publication. Furthermore, the Applicants respectfully request that the rejections of claims 1 and 2 be withdrawn.

B. 35 U.S.C. §103

1. Claims 3, 5-8, 11, 15, 16, 18-20

The Examiner rejected claims 3, 5-8, 11, 15, 16, 18-20 as being unpatentable over the Russ publication (United States patent publication 2002/0041007, published April 11, 2002). The rejection is respectfully traversed.

As the Russ publication was filed on October 10, 2001 and published on April 11, 2002, after the Applicants' November 5, 2001 filing date, the Russ publication is a 102(e) type reference. Russ is commonly assigned to Sarnoff Corporation, which was recorded on October 10, 2001 (Reel/Frame 012254/0569). The Applicants' invention is also assigned to Sarnoff Corporation, and was recorded on September 5, 2002 (Reel/Frame 013383/0743). The Applicants' invention and the Russ publication were, at the time Applicants' invention was made, owned by, or subject to an obligation of assignment to, Sarnoff Corporation. Since this application was filed after November 29, 1999, the Russ publication does not preclude patentability under the provisions of 35 U.S.C. §103(c), as amended by the American Inventors' Protection Act of 1999 (see, MPEP 706.02(l)(1)).

As such, the Applicants respectfully submit that claims 3, 5-8, 11, 15, 16, and 18-20 fully satisfy the requirements under 35 U.S.C. §103 and are patentable thereunder. Therefore, the Applicants respectfully request the foregoing rejections to claims 3, 5-8, 11, 15, 16, and 18-20 be withdrawn.

CONCLUSION

Thus, Applicants submit that none of the claims presently in the application are anticipated under the provisions of 35 U.S.C. §102, or obvious under the provisions of 35 U.S.C. §103. Consequently, Applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Mr. Steven Hertzberg at (732) 530-9404 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

8/29/03

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